Amendments to the Drawings:

The attached sheet of drawings include changes to Figure 1. The sheet, which includes Figure 1, replace the original sheet. Specifically, Figure 1 is amended to include the legend "PRIOR ART", which was missing from the original sheet.

A marked-up version of the drawing, with revisions shown in red, is included with the amended drawing. Entry of the amendments to the drawing is respectfully requested.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

Applicants affirm the election of Species A of claims 1-16, 23-25, and 27-29. Claims 17-22 and 26 are withdrawn from consideration as being drawn to non-elected species. However, Applicants note that the Office Action Summary states that claim 25 is withdrawn from consideration. Applicants believe that this is in error, in view of Applicants' Response to Species Election Requirement mailed on March 23, 2005, electing Group A, including claims 1-16, 24, and 25 corresponding to Figures 2-4, without traverse, and acknowledging claims 23 and 27-29 as generic.

The drawings are objected to under 37 CFR 1.83(a). Regarding the first and second internal voltage generation circuits set forth in claims 23, 24, and 27-29, these claims are amended such that all features set forth in the claims are shown in the drawings. Also, Figure 1 is amended to include the legend "Prior Art," as suggested in the Office Action at page 2, paragraph 3. Reconsideration of the objections to the drawings is respectfully requested.

Claims 23-24 are rejected under 35 U.S.C. 112. The claims are amended such that all features set forth in the claims include support in the specification and drawings. Reconsideration of the rejections of claims 23 and 24 under 35 U.S.C. 112 is respectfully requested.

Claims 4-6 and 13 are objected to, but would be allowable if rewritten in independent form. Applicants wish to defer submission of these claims in independent form, pending consideration of the present Amendment.

Claims 1-3, 7-12, 14-16, 23-24, and 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishita (U.S. Patent No. 6,184,744). It is believed that it was intended that claim 25 be included in this rejection, since, as noted above, it is believed that claim 25 should not be withdrawn. The following remarks therefore assume that claim 25 is included in the rejections. In view of the amendments to the claims and the following remarks, it is believed that the claims are allowable over the Morishita reference. Accordingly, reconsideration of the rejections is respectfully requested.

Applicants' invention is directed to an internal voltage generating circuit comprising a

control signal generating circuit, a comparing circuit, a driving signal control circuit, and an internal voltage driving circuit. The control signal generating circuit generates a control signal according to a number of data bits. The control signal is inactivated when the number of data bits is more than a predetermined number of bits, and the control signal is activated when the number of data bits is less than the predetermined number of bits. This feature is illustrated by way of example at least at Figure 2 of the present specification. In this example, the control signal generating circuit 20 generates a control signal C, which has a logic high level, i.e., activated, when the number of data bits that is provided to the semiconductor device exceeds a predetermined number of bits, and generates the control signal having a logic low level, i.e., inactivated, when the number of data bits is less than the predetermined number of bits (see Figure 2 and page 7, line 23 through page 8, line 3 of the present specification).

In addition, the comparing circuit is enabled for being provided an external power voltage as a power voltage when the control signal is activated, and comparing a reference voltage to an internal voltage to generate a driving signal. This feature is illustrated by way of example at least at Figure 2 of the present specification. In this example, when the control signal C is inactivated, the PMOS transistor P1 is turned on, whereby the comparator 10 receives an external power voltage EVC as a power voltage, and compares a reference voltage VREF to an internal voltage IVC to generate a driving signal (see Figure 2, page 2, lines 11-15, and page 8, lines 4-7 of the present specification).

The claims are amended herein to clarify certain details of the invention. In particular, independent claims 1, 10, and 23 are amended to specifically point out that the control signal is inactivated when the number of data bits is more than a predetermined number of bits, and the control signal is activated when the number of data bits is less than the predetermined number of bits. In addition, claim 1 is amended to clarify that the comparing circuit is enabled by being provided an external power voltage as a power voltage when the control signal is activated, and comparing a reference voltage to an internal voltage to generate a driving signal.

Morishita discloses an internal power supply voltage generation circuit that includes a level adjust circuit 1, an activation control circuit 2, and a main amplifier MA comprising a

comparator CMM (see Morishita, Figures 1-2). The level adjust circuit 1 of Morishita comprises a lower limit detection circuit 1a that detects an equalization of reference voltage Vref and external power supply voltage ExtVcc, and generates a lower detection signal SIG (see Morishita, Figures 2 and 4, and column 10, lines 20-24). The activation control circuit 2 generates an activation control signal ACT for determining the operating period of internal circuit 3 (see Morishita, Figures 1-2, column 9, lines 25-27).

It is submitted that Morishita fails to teach or suggest the present invention set forth in the amended claims. In particular, it is submitted that Morishita fails to teach or suggest a control signal generating circuit for generating a control signal according to a number of data bits, as claimed. The Office Action at page 3, paragraph 4 refers to the activation control signal ACT and lower detection signal SIG of Morishita as a number of data bits. However, there is no mention in Morishita of the ACT and SIG signals as being a number of data bits. Instead, the ACT signal is generated with reference to the operating period of the internal circuit 3, and the SIG signal is generated in accordance with the comparison result of a power supply voltage ExtVcc and reference voltage Vref (see Morishita, Figures 2 and 4, and column 12, lines 44-48). The Office Action at page 3, paragraph 4 further cites the AND circuit 1d of Morishita as Applicants' control signal generating circuit, and further cites the output of AND circuit 1d as the Applicant's cited control signal. However, since the AND circuit 1d generates an output based on the ACT and SIG signals as inputs to the AND circuit 1d, and since both the ACT and SIG signal function as independent signals, and not as the number of data bits, it follows that the AND circuit 1d of Morishita is not the control signal generating circuit of the present invention, and it follows that the output of AND circuit 1d is not the control signal of the present invention.

In addition, since Morishita fails to teach or suggest the control signal generating circuit and the control signal of the present invention, it follows that Morishita fails to teach or suggest a control signal that is inactivated when the number of data bits is more than a predetermined number of bits, and is activated when the number of data bits is less than the predetermined number of bits, as claimed. Moreover, there is no mention in Morishita of inactivating the output of AND circuit 1d (referred to in the Office Action as a control signal) when the number of data

bits is greater than a predetermined number of bits, or activating the output of AND circuit 1d when the number of bits is less than the predetermined number of bits.

In addition, with regard to independent claim 1, it is submitted that Morishita fails to teach or suggest that the comparing circuit that is enabled by being provided an external power voltage as a power voltage when the control signal is inactivated, as claimed. While Figure 2 of Morishita discloses the AND circuit 1d providing an output to the gate of a MOS transistor 1e, there is no mention in Morishita that the AND circuit 1d output enables the comparator CMM when the control signal is inactivated. For these reasons, the asserted AND circuit 1d output is different than the control signal of the present invention.

Therefore, it is submitted that Morishita fails to teach the invention set forth in the amended claims. Reconsideration of the rejections of claims 1-3, 7-12, 14-16, 23-25, and 27-29 under 35 U.S.C. 102(b) based on Morishita is therefore respectfully requested.

In view of the amendments to the claims and the foregoing remarks, it is believed that all claims pending in the application are in condition for allowance, and such allowance is respectfully solicited. If a telephone conference will expedite prosecution of the application, the Examiner is invited to telephone the undersigned.

Respectfully submitted,

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Steven M. Mills
Registration Number 36,610
Attorney for Applicants

Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900
Facsimile: (617) 742-7774
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FIG. 1
(PRIOR ART)